OPA858-Q1 5.5-GHz Gain Bandwidth Product, Gain of 7-V/V Stable, FET Input Amplifier

1 Features

- AEC-Q100 Qualified for Automotive Applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- High Gain Bandwidth Product: 5.5 GHz
- Decompensated, Gain ≥ 7 V/V (Stable)
- Ultra-Low Bias Current MOSFET Inputs: 10 pA
- Low Input Voltage Noise: 2.5 nV/\sqrt{Hz}
- Slew rate: 2000 V/µs
- Low Input Capacitance:
  - Common-Mode: 0.6 pF
  - Differential: 0.2 pF
- Wide Input Common-Mode Range:
  - 1.4 V from Positive Supply
  - Includes Negative Supply
- 2.5 Vpp Output Swing in TIA Configuration
- Supply Voltage Range: 3.3 V to 5.25 V
- Quiescent Current: 20.5 mA
- Package: 8-Pin WSON
- Temperature Range: –40°C to +125°C

2 Applications

- Automotive LIDAR
- Time of flight (ToF) Camera
- Optical Time Domain Reflectometry (OTDR)
- 3D Scanner
- Laser Distance Measurement
- Solid-State Scanning LIDAR
- Optical ToF Position Sensor
- Drone Vision
- Silicon Photomultiplier (SiPM) Buffer Amplifier
- Photomultiplier Tube Post Amplifier

3 Description

The OPA858-Q1 is a wideband, low-noise operational amplifier with CMOS inputs for wideband transimpedance and voltage amplifier applications. When the device is configured as a transimpedance amplifier (TIA), the 5.5-GHz gain bandwidth product (GBWP) enables high closed-loop bandwidths at transimpedance gains in the range of tens to hundreds of kΩs.

The graph below shows the bandwidth and noise performance of the OPA858-Q1 as a function of the photodiode capacitance when the amplifier is configured as a TIA. The total noise is calculated along a bandwidth range extending from DC to the calculated frequency (f) on the left scale. The OPA858-Q1 package has a feedback pin (FB) that simplifies the feedback network connection between the input and the output.

The OPA858-Q1 is optimized to operate in optical time-of-flight (ToF) systems where the OPA858-Q1 is used with time-to-digital converters, such as the TDC7201. Use the OPA858-Q1 to drive a high-speed analog-to-digital converter (ADC) in high-resolution LIDAR systems with a differential output amplifier, such as the THS4541-Q1.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER(1)</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA858-Q1</td>
<td>WSON (8)</td>
<td>2.00 mm × 2.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the package option addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
# Table of Contents

1 Features ................................................................. 1  
2 Applications ............................................................. 1  
3 Description ............................................................ 1  
4 Revision History ...................................................... 2  
5 Pin Configuration and Functions ............................... 4  
6 Specifications ........................................................ 5  
   6.1 Absolute Maximum Ratings .................................. 5  
   6.2 ESD Ratings ...................................................... 5  
   6.3 Recommended Operating Conditions ..................... 5  
   6.4 Thermal Information .......................................... 5  
   6.5 Electrical Characteristics .................................. 6  
   6.6 Typical Characteristics ..................................... 8  
7 Parameter Measurement Information ........................ 15  
8 Detailed Description ............................................... 16  
   8.1 Overview ........................................................ 16  
   8.2 Functional Block Diagram .................................. 16  
   8.3 Feature Description .......................................... 17  
   8.4 Device Functional Modes .................................. 20  
9 Application and Implementation .............................. 21  
   9.1 Application Information .................................... 21  
   9.2 Typical Application .......................................... 22  
10 Power Supply Recommendations ............................ 25  
11 Layout ................................................................. 26  
   11.1 Layout Guidelines ........................................... 26  
   11.2 Layout Example ............................................. 26  
12 Device and Documentation Support ........................ 28  
   12.1 Device Support ............................................... 28  
   12.2 Documentation Support ................................... 28  
   12.3 Receiving Notification of Documentation Updates .. 28  
   12.4 Support Resources ......................................... 28  
   12.5 Trademarks ................................................... 28  
   12.6 Electrostatic Discharge Caution ......................... 28  
   12.7 Glossary ........................................................ 28  
13 Mechanical, Packaging, and Orderable Information .. 28  
   13.1 Mechanical ................................................... 28  
   13.2 Packaging ..................................................... 28  
   13.3 Orderable ........................................................ 28  

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>February 2021</td>
<td>*</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>
## Device Comparison Table

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>INPUT TYPE</th>
<th>MINIMUM STABLE GAIN</th>
<th>VOLTAGE NOISE (nV/√Hz)</th>
<th>INPUT CAPACITANCE (pF)</th>
<th>GAIN BANDWIDTH (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA855-Q1</td>
<td>Bipolar</td>
<td>7 V/V</td>
<td>0.98</td>
<td>0.8</td>
<td>8</td>
</tr>
<tr>
<td>OPA858-Q1</td>
<td>CMOS</td>
<td>7 V/V</td>
<td>2.5</td>
<td>0.8</td>
<td>5.5</td>
</tr>
<tr>
<td>OPA859-Q1</td>
<td>CMOS</td>
<td>1 V/V</td>
<td>3.3</td>
<td>0.8</td>
<td>0.9</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

![Figure 5-1. DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View](image)

Table 5-1. Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB</td>
<td>1</td>
<td>I Feedback connection to output of amplifier</td>
</tr>
<tr>
<td>IN–</td>
<td>3</td>
<td>I Inverting input</td>
</tr>
<tr>
<td>IN+</td>
<td>4</td>
<td>I Noninverting input</td>
</tr>
<tr>
<td>NC</td>
<td>2</td>
<td>— Do not connect</td>
</tr>
<tr>
<td>OUT</td>
<td>6</td>
<td>O Amplifier output</td>
</tr>
<tr>
<td>PD</td>
<td>8</td>
<td>I Power down connection. PD = logic low = power off mode; PD = logic high = normal operation.</td>
</tr>
<tr>
<td>VS–</td>
<td>5</td>
<td>— Negative voltage supply</td>
</tr>
<tr>
<td>VS+</td>
<td>7</td>
<td>— Positive voltage supply</td>
</tr>
<tr>
<td>Thermal pad</td>
<td>—</td>
<td>Connect the thermal pad to VS–</td>
</tr>
</tbody>
</table>
6 Specifications
6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_S )</td>
<td>5.5</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{IN+}}, V_{\text{IN-}} )</td>
<td>( V_{\text{S-}} - 0.5 )</td>
<td>( (V_{\text{S+}} + 0.5) )</td>
<td>( V )</td>
</tr>
<tr>
<td>( V_{\text{ID}} )</td>
<td>1</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{OUT}} )</td>
<td>( V_{\text{S-}} - 0.5 )</td>
<td>( (V_{\text{S+}} + 0.5) )</td>
<td>( V )</td>
</tr>
<tr>
<td>( I_{\text{IN}} )</td>
<td>( \pm 10 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{OUT}} )</td>
<td>( \pm 100 )</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( T_J )</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>( T_A )</td>
<td>(-40)</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{\text{stg}} )</td>
<td>(-65)</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{ESD}} )</td>
<td>Human-body model (HBM), per AEC Q100-002(1)</td>
<td>( \pm 1500 )</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>( \pm 1000 )</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_S )</td>
<td>3.3</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>( T_A )</td>
<td>(-40)</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA858-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\text{JA}} )</td>
<td>Junction-to-ambient thermal resistance</td>
<td>80.1</td>
</tr>
<tr>
<td>( R_{\text{JC}(\text{top})} )</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>100</td>
</tr>
<tr>
<td>( R_{\text{JB}} )</td>
<td>Junction-to-board thermal resistance</td>
<td>45</td>
</tr>
<tr>
<td>( \Psi_{\text{JT}} )</td>
<td>Junction-to-top characterization parameter</td>
<td>6.8</td>
</tr>
<tr>
<td>( \Psi_{\text{JB}} )</td>
<td>Junction-to-board characterization parameter</td>
<td>45.2</td>
</tr>
<tr>
<td>( R_{\text{JC}(\text{bot})} )</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>22.7</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

\( V_{S+} = 5 \text{ V}, \ V_{S-} = 0 \text{ V}, \ G = 7 \text{ V/V}, R_F = 453 \Omega, \) input common-mode biased at midsupply, \( R_L = 200 \Omega, \) output load is referenced to midsupply, and \( T_A = 25^\circ \text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>AC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSBW Small-signal bandwidth</td>
<td>( V_{OUT} = 100 \text{ mV}_{PP} )</td>
<td>1.2</td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>LSBW Large-signal bandwidth</td>
<td>( V_{OUT} = 2 \text{ V}_{PP} )</td>
<td>600</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>GBWP Gain-bandwidth product</td>
<td>Bandwidth for 0.1-dB flatness</td>
<td>130</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>SR Slew rate (10% - 90%)</td>
<td>( V_{OUT} = 2 \text{-V step} )</td>
<td>2000</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>( t_r ) Rise time</td>
<td>( V_{OUT} = 100\text{-mV step} )</td>
<td>0.3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_f ) Fall time</td>
<td>( V_{OUT} = 100\text{-mV step} )</td>
<td>0.3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Settling time to 0.1%</td>
<td>( V_{OUT} = 2 \text{-V step} )</td>
<td>8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Settling time to 0.001%</td>
<td>( V_{OUT} = 2 \text{-V step} )</td>
<td>3000</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Overshoot or undershoot</td>
<td>( V_{OUT} = 2 \text{-V step} )</td>
<td>7</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Overdrive recovery</td>
<td>2x output overdrive (0.1% recovery)</td>
<td>200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>HD2 Second-order harmonic distortion</td>
<td>( f = 10 \text{ MHz}, V_{OUT} = 2 \text{ V}_{PP} )</td>
<td>88</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td>( f = 100 \text{ MHz}, V_{OUT} = 2 \text{ V}_{PP} )</td>
<td>64</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>HD3 Third-order harmonic distortion</td>
<td>( f = 10 \text{ MHz}, V_{OUT} = 2 \text{ V}_{PP} )</td>
<td>86</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td>( f = 100 \text{ MHz}, V_{OUT} = 2 \text{ V}_{PP} )</td>
<td>68</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>( e_n ) Input-referred voltage noise</td>
<td>( f = 1 \text{ MHz} )</td>
<td>2.5</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>( Z_{OUT} ) Closed-loop output impedance</td>
<td>( f = 1 \text{ MHz} )</td>
<td>0.15</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td><strong>DC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( A_{OL} ) Open-loop voltage gain</td>
<td></td>
<td>72</td>
<td>75</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( V_{OS} ) Input offset voltage</td>
<td>( T_A = 25^\circ \text{C} )</td>
<td>–5</td>
<td>±0.8</td>
<td>5</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta V_{OS}/\Delta T ) Input offset voltage drift</td>
<td>( T_A = –40^\circ \text{C to } +125^\circ \text{C} )</td>
<td>±2</td>
<td></td>
<td></td>
<td>μV/°C</td>
</tr>
<tr>
<td>( I_{B0N}, I_{BI} ) Input bias current</td>
<td>( T_A = 25^\circ \text{C} )</td>
<td>±0.4</td>
<td></td>
<td>5</td>
<td>pA</td>
</tr>
<tr>
<td>( I_{BOS} ) Input offset current</td>
<td>( T_A = 25^\circ \text{C} )</td>
<td>±0.01</td>
<td>5</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>CMRR Common-mode rejection ratio</td>
<td>( V_{CM} = ±0.5 \text{ V}, ) referenced to midsupply</td>
<td>70</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-mode input resistance</td>
<td></td>
<td>1</td>
<td></td>
<td>GΩ</td>
<td></td>
</tr>
<tr>
<td>Common-mode input capacitance</td>
<td></td>
<td>0.62</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Differential input resistance</td>
<td></td>
<td>1</td>
<td></td>
<td>GΩ</td>
<td></td>
</tr>
<tr>
<td>Differential input capacitance</td>
<td></td>
<td>0.2</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>( V_{IH} ) Common-mode input range (high)</td>
<td>CMRR &gt; 66 dB, ( V_{S+} = 3.3 \text{ V} )</td>
<td>1.7</td>
<td>1.9</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} ) Common-mode input range (low)</td>
<td>CMRR &gt; 66 dB, ( V_{S+} = 3.3 \text{ V} )</td>
<td>0</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} ) Common-mode input range (high)</td>
<td>CMRR &gt; 66 dB</td>
<td>3.4</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} ) Common-mode input range (low)</td>
<td>CMRR &gt; 66 dB</td>
<td>0</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OH} ) Output voltage (high)</td>
<td>( T_A = 25^\circ \text{C}, \ V_{S+} = 3.3 \text{ V} )</td>
<td>2.3</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OH} ) Output voltage (high)</td>
<td>( T_A = 25^\circ \text{C} )</td>
<td>3.95</td>
<td>4.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} ) Output voltage (low)</td>
<td>( T_A = –40^\circ \text{C to } +125^\circ \text{C} )</td>
<td>3.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} ) Output voltage (low)</td>
<td>( T_A = 25^\circ \text{C}, \ V_{S+} = 3.3 \text{ V} )</td>
<td>1.05</td>
<td>1.15</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} ) Output voltage (low)</td>
<td>( T_A = –40^\circ \text{C to } +125^\circ \text{C} )</td>
<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
6.5 Electrical Characteristics (continued)

\( V_{S+} = 5 \, \text{V}, \, V_{S-} = 0 \, \text{V}, \, G = 7 \, \text{V/V}, \, R_F = 453 \, \Omega, \) input common-mode biased at midsupply, \( R_L = 200 \, \Omega, \) output load is referenced to midsupply, and \( T_A = 25^\circ \text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear output drive (sink and source)</td>
<td>( R_L = 10 , \Omega, , A_{OL} &gt; 60 , \text{dB} )</td>
<td>65</td>
<td>80</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( T_A = -40^\circ \text{C} ) \text{to} +125^\circ \text{C}, , R_L = 10 , \Omega, , A_{OL} &gt; 60 , \text{dB} )</td>
<td>64</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SC} ) Output short-circuit current</td>
<td></td>
<td>85</td>
<td>105</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**POWER SUPPLY**

| \( V_S \) Operating voltage       |                                    | 3.3 | 5.25 | V    |
| \( I_Q \) Quiescent current \( V_{S+} = 5 \, \text{V} \) |                                    | 18  | 20.5 | 24  | mA   |
| \( I_Q \) Quiescent current \( V_{S+} = 3.3 \, \text{V} \) |                                    | 17.5| 20   | 23.5| mA   |
| \( I_Q \) Quiescent current \( V_{S+} = 5.25 \, \text{V} \) |                                    | 18  | 21   | 24  | mA   |
| \( I_Q \) Quiescent current \( T_A = 125^\circ \text{C} \) |                                    |     | 24.5 |     | mA   |
| \( I_Q \) Quiescent current \( T_A = -40^\circ \text{C} \) |                                    |     | 18.5 |     | mA   |
| \( V_{SC} \) Positive power-supply rejection ratio |                                    | 74  | 84   |     | dB   |
| \( I_{Q+} \) Negative power-supply rejection ratio |                                    | 70  | 80   |     |      |

**POWER DOWN**

| Disable voltage threshold | Ampifier OFF below this voltage | 0.65 | 1  | V    |
| Enable voltage threshold | Ampifier ON above this voltage  | 1.5  | 1.8| V    |
| Power-down quiescent current |                              | 70  | 140| µA   |
| PD bias current |                                    | 70  | 200| µA   |
| Turnon time delay | Time to \( V_{OUT} = 90\% \) of final value | 13  |     | ns   |
| Turnoff time delay |                                    | 120 |     | ns   |
6.6 Typical Characteristics

at $V_{S+} = 2.5 \, \text{V}$, $V_{S-} = -2.5 \, \text{V}$, $V_{IN+} = 0 \, \text{V}$, $R_F = 453 \, \Omega$, Gain = 7 V/V, $R_L = 200 \, \Omega$, output load referenced to midsupply, and $T_A = 25^\circ\text{C} \text{ (unless otherwise noted)}$

$V_{OUT} = 100 \, \text{mV}_{\text{PP}}$; see Figure 7-1 and Figure 7-2 for circuit configuration

Figure 6-1. Small-Signal Frequency Response vs Gain

$V_{OUT} = 100 \, \text{mV}_{\text{PP}}$

Figure 6-2. Small-Signal Frequency Response vs Supply Voltage

$V_{OUT} = 100 \, \text{mV}_{\text{PP}}$

Figure 6-3. Small-Signal Frequency Response vs Output Load

$V_{OUT} = 100 \, \text{mV}_{\text{PP}}$

Figure 6-4. Small-Signal Frequency Response vs Ambient Temperature

$V_{OUT} = 100 \, \text{mV}_{\text{PP}}$

Figure 6-5. Small-Signal Frequency Response vs Capacitive Load

$V_{OUT} = 100 \, \text{mV}_{\text{PP}}$; see Figure 7-3 for circuit configuration

Figure 6-6. Large-Signal Frequency Response vs Gain

$V_{OUT} = 2 \, \text{V}_{\text{PP}}$
6.6 Typical Characteristics (continued)

at \( V_{S+} = 2.5 \text{ V}, V_{S-} = -2.5 \text{ V}, V_{IN+} = 0 \text{ V}, R_F = 453 \text{ } \Omega, \) Gain = 7 \( \text{ V/V}, R_L = 200 \text{ } \Omega, \) output load referenced to midsupply, and \( T_A = 25^\circ \text{C} \) (unless otherwise noted)

![Image of normalized gain vs frequency]

**Figure 6-7. Large-Signal Response for 0.1-dB Gain Flatness**

![Image of frequency response]

**Figure 6-8. Large-Signal Frequency Response**

![Image of closed-loop output impedance vs frequency]

**Figure 6-9. Closed-Loop Output Impedance vs Frequency**

![Image of open-loop magnitude and phase vs frequency]

**Figure 6-10. Open-Loop Magnitude and Phase vs Frequency**

![Image of voltage noise density vs frequency]

**Figure 6-11. Voltage Noise Density vs Frequency**

![Image of voltage noise density vs ambient temperature]

**Figure 6-12. Voltage Noise Density vs Ambient Temperature**
6.6 Typical Characteristics (continued)

at \( V_{S^+} = 2.5 \text{ V}, V_{S^-} = -2.5 \text{ V}, V_{\text{IN}^+} = 0 \text{ V}, R_F = 453 \Omega, \text{ Gain} = 7 \text{ V/V}, R_L = 200 \Omega, \) output load referenced to midsupply, and \( T_A = 25^\circ \text{C} \) (unless otherwise noted)
6.6 Typical Characteristics (continued)

at \( V_{S+} = 2.5 \text{ V, } V_{S-} = -2.5 \text{ V, } V_{IN+} = 0 \text{ V, } R_F = 453 \text{ }\Omega \), Gain = 7 V/V, \( R_L = 200 \text{ }\Omega \), output load referenced to midsupply, and \( T_A = 25^\circ\text{C} \) (unless otherwise noted)

Average Rise and Fall Time (10% - 90%) = 450 ps

Average Rise and Fall Time (10% - 90%) = 750 ps

**Figure 6-19. Small-Signal Transient Response**

**Figure 6-20. Large-Signal Transient Response**

**Figure 6-21. Small-Signal Transient Response vs Capacitive Load**

**Figure 6-22. Output Overload Response**

**Figure 6-23. Turnon Transient Response**

**Figure 6-24. Turnoff Transient Response**
6.6 Typical Characteristics (continued)

at $V_{S+} = 2.5\, V$, $V_{S-} = -2.5\, V$, $V_{IN+} = 0\, V$, $R_F = 453\, \Omega$, Gain = 7 V/V, $R_L = 200\, \Omega$, output load referenced to midsupply, and $T_A = 25^\circ C$ (unless otherwise noted).

---

### Figure 6-25. Common-Mode Rejection Ratio vs Frequency

- Common-Mode Rejection Ratio (dB) vs Frequency (Hz)
- 2 Typical Units

### Figure 6-26. Power Supply Rejection Ratio vs Frequency

- Power Supply Rejection Ratio (dB) vs Frequency (Hz)
- 2 Typical Units

### Figure 6-27. Quiescent Current vs Supply Voltage

- Quiescent Current (mA) vs Total Supply Voltage (V)
- 2 Typical Units

### Figure 6-28. Quiescent Current vs Ambient Temperature

- Quiescent Current (mA) vs Ambient Temperature (°C)
- 2 Typical Units

### Figure 6-29. Quiescent Current (Amplifier Disabled) vs Ambient Temperature

- Quiescent Current (UA) vs Ambient Temperature (°C)
- 30 Units Tested

### Figure 6-30. Offset Voltage vs Supply Voltage

- Offset Voltage (mV) vs Total Supply Voltage (V)
- 3 Typical Units
6.6 Typical Characteristics (continued)

at \( V_{S+} = 2.5 \text{ V}, V_{S-} = -2.5 \text{ V}, V_{IN+} = 0 \text{ V}, R_F = 453 \Omega, \text{Gain} = 7 \text{ V/V}, R_L = 200 \Omega, \) output load referenced to midsupply, and \( T_A = 25^\circ\text{C} \) (unless otherwise noted)

\[
\mu = 1 \mu\text{V/}^\circ\text{C} \quad \sigma = 2.2 \mu\text{V/}^\circ\text{C} \quad 28 \text{ Units Tested}
\]

Figure 6-31. Offset Voltage vs Ambient Temperature

\( V_S = 3.3 \text{ V} \quad 3 \text{ Typical Units} \)

Figure 6-32. Offset Voltage vs Input Common-Mode Voltage

\( V_S = 5 \text{ V} \quad 3 \text{ Typical Units} \)

Figure 6-33. Offset Voltage vs Input Common-Mode Voltage

\( V_S = 3.3 \text{ V} \quad 3 \text{ Typical Units} \)

Figure 6-34. Offset Voltage vs Input Common-Mode Voltage vs Ambient Temperature

\( V_S = 5 \text{ V} \quad 3 \text{ Typical Units} \)

Figure 6-35. Offset Voltage vs Output Swing

\( V_S = 3.3 \text{ V} \quad 3 \text{ Typical Units} \)

Figure 6-36. Offset Voltage vs Output Swing
6.6 Typical Characteristics (continued)

at \( V_{S+} = 2.5 \, \text{V} \), \( V_{S-} = -2.5 \, \text{V} \), \( V_{\text{IN}+} = 0 \, \text{V} \), \( R_F = 453 \, \text{Ω} \), Gain = 7 \( \text{V/V} \), \( R_L = 200 \, \text{Ω} \), output load referenced to midsupply, and \( T_A = 25^\circ \text{C} \) (unless otherwise noted)

---

**Figure 6-37. Offset Voltage vs Output Swing vs Ambient Temperature**

**Figure 6-38. Input Bias Current vs Ambient Temperature**

**Figure 6-39. Input Bias Current vs Input Common-Mode Voltage**

**Figure 6-40. Quiescent Current Distribution**

**Figure 6-41. Offset Voltage Distribution**

**Figure 6-42. Input Bias Current Distribution**
7 Parameter Measurement Information

The various test setup configurations for the OPA858-Q1 are shown in Figure 7-1, Figure 7-2, and Figure 7-3. When configuring the OPA858-Q1 in a gain of +39.2 V/V, feedback resistor $R_F$ was set to 953 Ω.

Figure 6-1 shows 5-dB of peaking with the amplifier in an inverting configuration of –7 V/V with the amplifier configured as shown in Figure 7-2. The 50-Ω matched termination of this circuit configuration results in the amplifier being configured in a noise gain of 5.3 V/V, which is lower than the recommended +7 V/V.

![Figure 7-1. Noninverting Configuration](image1)

$R_o$ values depend on gain configuration

![Figure 7-2. Inverting Configuration (Gain = –7 V/V)](image2)

![Figure 7-3. Capacitive Load Driver Configuration](image3)
8 Detailed Description

8.1 Overview

The ultra-wide, 5.5-GHz gain bandwidth product (GBWP) of the OPA858-Q1, combined with the broadband voltage noise of 2.5 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA858-Q1 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA858-Q1 has 600 MHz of large-signal bandwidth (\(V_{\text{OUT}} = 2V_{\text{PP}}\)), and a slew rate of 2000 V/μs.

The OPA858-Q1 is offered in a 2-mm × 2-mm, 8-pin WSON package that features a feedback (FB) pin for a simple feedback network connection between the amplifiers output and inverting input. Excess capacitance on an amplifiers input pin can reduce phase margin causing instability. This problem is exacerbated in the case of very wideband amplifiers like the OPA858-Q1. To reduce the effects of stray capacitance on the input node, the OPA858-Q1 pinout features an isolation pin (NC) between the feedback and inverting input pins that increases the physical spacing between them thereby reducing parasitic coupling at high frequencies. The OPA858-Q1 also features a very low capacitance input stage with only 0.8-pF of total input capacitance.

8.2 Functional Block Diagram

The OPA858-Q1 is a classic voltage feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, like the two basic options shown in Figure 8-1 and Figure 8-2. The DC operating point for each configuration is level-shifted by the reference voltage (\(V_{\text{REF}}\)), which is typically set to midsupply in single-supply operation. \(V_{\text{REF}}\) is typically connected to ground in split-supply applications.
8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA858-Q1 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as Figure 8-3 shows. There are two antiparallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

![Figure 8-3. Internal ESD Structure](image)

8.3.2 Feedback Pin

The OPA858-Q1 pin layout is optimized to minimize parasitic inductance and capacitance, which is a critical care about in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor ($R_F$) can connect between the FB and IN– pin on the same side of the package (see Figure 8-4) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins by increasing the physical separation between the pins.

![Figure 8-4. $R_F$ Connection Between FB and IN– Pins](image)
8.3.3 Wide Gain-Bandwidth Product

Figure 6-10 shows the open-loop magnitude and phase response of the OPA858-Q1. Calculate the gain bandwidth product of any op amp by determining the frequency at which the $A_{OL}$ is 60 dB and multiplying that frequency by a factor of 1000. The second pole in the $A_{OL}$ response occurs before the magnitude crosses 0 dB, and the resultant phase margin is less than 0°. This indicates instability at a gain of 0 dB (1 V/V). Amplifiers that are not unity-gain stable are known as decompensated amplifiers. Decompensated amplifiers typically have higher gain-bandwidth product, higher slew rate, and lower voltage noise, compared to a unity-gain stable amplifier with the same amount of quiescent power consumption.

Figure 8-5 shows the open-loop magnitude ($A_{OL}$) of the OPA858-Q1 as a function of temperature. The results show minimal variation over temperature. The phase margin of the OPA858-Q1 configured in a noise gain of 7 V/V (16.9 dB) is close to 55° across temperature. Similarly Figure 8-6 shows the $A_{OL}$ magnitude of the OPA858-Q1 as a function of process variation. The results show the $A_{OL}$ curve for the nominal process corner and the variation one standard deviation from the nominal. The simulated results suggest less than 1° of phase margin difference within a standard deviation of process variation when the amplifier is configured in a gain of 7 V/V.

One of the primary applications for the OPA858-Q1 is as a high-speed transimpedance amplifier (TIA), as Figure 9-4 shows. The low-frequency noise gain of a TIA is 0 dB (1 V/V). At high frequencies the ratio of the total input capacitance and the feedback capacitance set the noise gain. To maximize the TIA closed-loop bandwidth, the feedback capacitance is typically smaller than the input capacitance, which implies that the high-frequency noise gain is greater than 0 dB. As a result, op amps configured as TIAs are not required to be unity-gain stable, which makes a decompensated amplifier a viable option for a TIA. What You Need To Know About Transimpedance Amplifiers – Part 1 and What You Need To Know About Transimpedance Amplifiers – Part 2 describe transimpedance amplifier compensation in greater detail.
8.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA858-Q1 features a high slew rate of 2000 V/µs. The slew rate is a critical parameter in high-speed pulse applications with narrow sub-10-ns pulses, such as optical time-domain reflectometry (OTDR) and LiDAR. The high slew rate of the OPA858-Q1 implies that the device accurately reproduces a 2-V, sub-ns pulse edge, as seen in Figure 6-20. The wide bandwidth and slew rate of the OPA858-Q1 make it an excellent amplifier for high-speed signal-chain front ends.

Figure 8-7 shows the open-loop output impedance of the OPA858-Q1 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA858-Q1 is limited to approximately 3 V. The OPA858-Q1 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA858-Q1 output swing range coupled with the class-leading voltage noise specification for a CMOS amplifier maximizes the overall dynamic range of the signal chain.

![Figure 8-7. Open-Loop Output Impedance (Z_{OL}) vs Frequency](image)

8.3.5 Current Noise

The input impedance of CMOS and JFET input amplifiers at low frequencies exceed several GΩs. However, at higher frequencies, the transistors parasitic capacitance to the drain, source, and substrate reduces the impedance. The high impedance at low frequencies eliminates any bias current and the associated shot noise. At higher frequencies, the input current noise increases (see Figure 8-8) as a result of capacitive coupling between the CMOS gate oxide and the underlying transistor channel. This phenomenon is a natural artifact of the construction of the transistor and is unavoidable.

![Figure 8-8. Input Current Noise (I_{BN} and I_{BI}) vs Frequency](image)
8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA858-Q1 can be configured with single-sided supplies or split-supplies as shown in Figure 10-1. Split-supply operation using balanced supplies with the input common-mode set to ground eases lab testing because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground. In split-supply operation, the thermal pad must be connected to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA858-Q1 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. In single-supply operation, level shift the DC input and output reference voltages by half the difference between the power supply rails. This configuration maintains the input common-mode and output load reference at mid-supply. To eliminate gain errors, the source driving the reference input common-mode voltage must have low output impedance across the frequency range of interest. In this case, the thermal pad must be connected to ground.

8.4.2 Power-Down Mode

The OPA858-Q1 features a power-down mode to reduce the quiescent current to conserve power. Figure 6-23 and Figure 6-24 show the transient response of the OPA858-Q1 as the PD pin toggles between the disabled and enabled states.

The PD disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable and enable threshold voltages are 0.65 V and 1.8 V, respectively. If the amplifier is configured with ±1.65 V supplies, then the threshold voltages are at –1 V and 0.15 V. If the amplifier is configured with ±2.5 V supplies, then the threshold voltages are at –1.85 V and –0.7 V.

Figure 8-9 shows the switching behavior of a typical amplifier as the PD pin is swept down from the enabled state to the disabled state. Similarly, Figure 8-10 shows the switching behavior of a typical amplifier as the PD pin is swept up from the disabled state to the enabled state. The small difference in the switching thresholds between the down sweep and the up sweep is caused by the hysteresis designed into the amplifier to increase immunity to noise on the PD pin.

Connecting the PD pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (RF) and gain (RG) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA858-Q1 uses internal, back-to-back protection diodes between the inverting and noninverting input pins as Figure 8-3 shows. In the power-down state, if the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the noninverting input pin and the output pin.
9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Using the OPA858-Q1 as a Transimpedance Amplifier

The OPA858-Q1 design has been optimized to meet the industry’s growing demand for wideband, low-noise photodiode amplifiers. The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

1. The total input capacitance. This includes the photodiode capacitance, input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.
2. The op amp gain bandwidth product (GBWP), and,
3. The transimpedance gain $R_F$.

![Transimpedance Amplifier Circuit Diagram]

Figure 9-1. Transimpedance Amplifier Circuit

Figure 9-1 shows the OPA858-Q1 configured as a TIA with the avalanche photodiode (APD) reverse biased such that the APD cathode is tied to a large positive bias voltage. In this configuration the APD sources current into the op amp feedback loop so that the output swings in a negative direction relative to the input common-mode voltage. To maximize the output swing in the negative direction, the OPA858-Q1 common-mode is set close to the positive limit, 1.6 V from the positive supply rail.

The feedback resistance $R_F$ and the input capacitance form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted by adding the feedback capacitor ($C_F$) into the noise gain transfer function. The Transimpedance Considerations for High-Speed Amplifiers application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular gain and input capacitance. The bandwidth and compensation equations from the application report are available in a Microsoft Excel® calculator. What You Need To Know About Transimpedance Amplifiers – Part 1 provides a link to the calculator.
The equations and calculators in the application report and blog posts referenced above are used to model the bandwidth (f_{-3dB}) and noise (I_{RN}) performance of the OPA858-Q1 configured as a TIA. The resultant performance is shown in Figure 9-2 and Figure 9-3. The left side Y-axis shows the closed-loop bandwidth performance, while the right side of the graph shows the integrated input referred noise. The noise bandwidth to calculate I_{RN}, for a fixed R_F and C_{PD} is set equal to the f_{-3dB} frequency.

Figure 9-2 shows the amplifier performance as a function of photodiode capacitance (C_{PD}) for R_F = 10 kΩ and 20 kΩ. Increasing C_{PD} decreases the closed-loop bandwidth. It is vital to reduce any stray parasitic capacitance from the PCB to maximize bandwidth. The OPA858-Q1 is designed with 0.8 pF of total input capacitance to minimize the effect on system performance.

Figure 9-3 shows the amplifier performance as a function of R_F for C_{PD} = 1 pF and 2 pF. Increasing R_F results in lower bandwidth. To maximize the signal-to-noise ratio (SNR) in an optical front-end system, maximize the gain in the TIA stage. Increasing R_F by a factor of X increases the signal level by X, but only increases the resistor noise contribution by \sqrt{X}, thereby improving SNR.

### 9.2 Typical Application

The high GBWP, low input voltage noise and high slew rate of the OPA858-Q1 makes the device a viable wideband, high input impedance voltage amplifier.

![Figure 9-4. OPA858-Q1 in a Gain of –2V/V (No Noise Gain Shaping)](image-url)
9.2.1 Design Requirements

Design a high-bandwidth, high-gain, voltage amplifier with the design requirements listed in Table 9-1. An inverting amplifier configuration is chosen here; however, the theory is applicable to a noninverting configuration as well. In an inverting configuration the signal gain and noise gain transfer functions are not equal, unlike the noninverting configuration.

Table 9-1. Design Requirements

<table>
<thead>
<tr>
<th>TARGET BANDWIDTH (MHz)</th>
<th>SIGNAL GAIN (V/V)</th>
<th>FEEDBACK RESISTANCE (Ω)</th>
<th>FREQUENCY PEAKING (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 750</td>
<td>–2</td>
<td>453</td>
<td>&lt; 2</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

The OPA858-Q1 is compensated to have less than 1 dB of peaking in a gain of 7 V/V. Using the device in lower gains results in increased peaking and potential instability. Figure 9-4 shows the OPA858-Q1 configured in a signal gain of –2 V/V. The DC noise gain (1/β) of the amplifier is affected by the 62-Ω termination resistor and the 50-Ω source resistor and is given by Equation 1. At higher frequencies the noise gain is affected by reactive elements such as inductors and capacitors. These include both discrete board components as well as printed circuit board (PCB) parasitics.

\[
\text{Noise Gain} = \frac{1}{\beta} = \left(1 + \frac{453 \Omega}{226 \Omega + (62 \Omega \parallel 50 \Omega)}\right) = 2.79 \text{ V/V} = 5.04 \text{ dB}
\]  

(1)

The stability and phase margin of the amplifier depend on the loop gain of the amplifier, which is the product of the A_{OL} and the feedback factor (β) of the amplifier. The β of a negative-feedback loop system is the portion of the output signal that is fed back to the input, and in the case of an amplifier is the inverse of the noise gain. The noise gain of the amplifier at high frequencies can be increased by adding an input capacitor and a feedback capacitor as Figure 9-5 shows. If done carefully, increasing 1/β improves the phase margin just as any amplifier is more stable in a high gain configuration versus a unity-gain buffer configuration. The modified network with the added capacitors alters the high-frequency noise gain, but does not alter the signal gain. The AN-1604 Decompensated Operational Amplifiers application report provides a detailed analysis of noise gain-shaping techniques for decompensated amplifiers and shows how to choose external resistors and capacitor values.

Figure 9-6 shows the uncompensated frequency response of the OPA858-Q1 configured as shown in Figure 9-4. Without any added noise gain shaping components, the OPA858-Q1 shows approximately 13 dB of peaking.

Figure 9-7 shows the noise gain compensated frequency response of the OPA858-Q1 configured as shown in Figure 9-5. The noise gain shaping elements reduce the peaking to less than 1.5 dB. The 2.7-pF input capacitor, the input capacitance of the amplifier, the gain resistor, and the feedback resistor create a zero in the noise gain at a frequency f, as Equation 2 shows.

\[
f = \frac{1}{2\pi(R_F \parallel R_G)C_{IN}}
\]  

(2)
where

- $R_F$ is the feedback resistor
- $R_G$ is the input or gain resistor (includes the effect of the source and termination resistor)
- $C_{IN}$ is the total input capacitance, which includes the external 2.7-pF capacitor, the amplifier input capacitance, and any parasitic PCB capacitance.

The zero in Equation 2 increases the noise gain at higher frequencies, which is important when compensating a decompensated amplifier. However, the noise gain zero reduces the loop gain phase which results in a lower phase margin. To counteract the phase reduction due to the noise gain zero, add a pole to the noise gain curve by inserting the 0.5-pF feedback capacitor. The pole occurs at a frequency shown in Equation 3. The noise gain pole and zero locations must be selected so that the rate-of-closure between the magnitude curves of $A_{OL}$ and $1/\beta$ is approximately 20 dB. To ensure this, the noise gain pole must occur before the $1/\beta$ magnitude curve intersects the $A_{OL}$ magnitude curve. In other words, the noise gain pole must occur before $|A_{OL}| = |1/\beta|$. The point at which the two curves intersect is known as the loop gain crossover frequency.

$$f = \frac{1}{2\pi R_F C_F}$$  \hspace{1cm} (3)

where

- $C_F$ is the feedback capacitor (includes any added PCB parasitic)

For more information on op amp stability, watch the *TI Precision Lab series on stability* video.
9.2.3 Application Curves

![Application Curves](image)

**Figure 9-6. Gain = –2 V/V, Uncompensated Frequency Response**

**Figure 9-7. Gain = –2 V/V, Compensated Frequency Response**

10 Power Supply Recommendations

The OPA858-Q1 operates on supplies from 3.3 V to 5.25 V. The OPA858-Q1 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA858-Q1 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

- **a) Single supply configuration**

  ![Single Supply Configuration](image)

- **b) Split supply configuration**

  ![Split Supply Configuration](image)

**Figure 10-1. Split and Single Supply Circuit Configuration**
11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA858-Q1 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.

- **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).

- **Careful selection and placement of external components preserves the high-frequency performance of the OPA858-Q1.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA858-Q1 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because \( R_F \) and \( R_G \) become part of the output load network of the amplifier.

11.2 Layout Example

![Representative schematic](image)

- Ground and power plane exist on inner layers.
- Ground and power plane removed from inner layers. Ground fill on outer layers also removed.

![Connect PD to VS+ to enable the amplifier](image)

- NC (Pin 2) isolates the IN- and FB pins thereby reducing capacitive coupling.
- Place gain and feedback resistors close to pins to minimize stray capacitance.
- Connect the thermal pad to the negative supply pin.

![Place bypass capacitor close to power pins](image)

**Figure 11-1. Layout Recommendation**
When configuring the OPA858-Q1 as a transimpedance amplifier additional care must be taken to minimize the inductance between the avalanche photodiode (APD) and the amplifier. Always place the photodiode on the same side of the PCB as the amplifier. Placing the amplifier and the APD on opposite sides of the PCB increases the parasitic effects due to via inductance. APD packaging can be quite large which often requires the APD to be placed further away from the amplifier than ideal. The added distance between the two device results in increased inductance between the APD and op amp feedback network as shown in Figure 11-2. The added inductance is detrimental to a decompensated amplifiers stability since it isolates the APD capacitance from the noise gain transfer function. The noise gain is given by Equation 4. The added PCB trace inductance between the feedback network increases the denominator in Equation 4 thereby reducing the noise gain and the phase margin. In cases where a leaded APD in a TO can is used inductance should be further minimized by cutting the leads of the TO can as short as possible.

The layout shown in Figure 11-2 can be improved by following some of the guidelines shown in Figure 11-3. The two key rules to follow are:

• Add an isolation resistor $R_{\text{ISO}}$ as close as possible to the inverting input of the amplifier. Select the value of $R_{\text{ISO}}$ to be between 10 $\Omega$ and 20 $\Omega$. The resistor dampens the potential resonance caused by the trace inductance and the amplifiers internal capacitance.

• Close the loop between the feedback elements ($R_F$ and $C_F$) and $R_{\text{ISO}}$ as close to the APD pins as possible. This ensures a more balanced layout and reduces the inductive isolation between the APD and the feedback network.

\[
\text{Noise Gain} = \left(1 + \frac{Z_F}{Z_{\text{IN}}} \right)
\]

(4)

where

• $Z_F$ is the total impedance of the feedback network.

• $Z_{\text{IN}}$ is the total impedance of the input network.
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- LIDAR Pulsed Time of Flight Reference Design
- LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters
- Wide Bandwidth Optical Front-end Reference Design

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, OPA858EVM user's guide
- Texas Instruments, Training Video: High-Speed Transimpedance Amplifier Design Flow
- Texas Instruments, Training Video: How to Design Transimpedance Amplifier Circuits
- Texas Instruments, Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model
- Texas Instruments, Transimpedance Considerations for High-Speed Amplifiers application report
- Texas Instruments, What You Need To Know About Transimpedance Amplifiers – Part 1
- Texas Instruments What You Need To Know About Transimpedance Amplifiers – Part 2

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

® is a registered trademark of Microsoft Corporation.

All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA858QDSGRQ1</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>858Q</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSCOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA858-Q1:

Addendum-Page 1
• Catalog: OPA858

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product
### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA858QDSGRQ1</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.3</td>
<td>2.3</td>
<td>1.15</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

![Tape and Reel Box Diagram](image)

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA858QDSGRO1</td>
<td>WSON</td>
<td>DSG</td>
<td>8</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated